```
 * * * * * * * * * * * * * * * * * * * * * * * * * * * * * * *
  *         U. S.   P A T E N T   T E X T   F I L E             *
  *                                                             *
  *  THE WEEKLY PATENT TEXT AND IMAGE DATA IS CURRENT           *
  *  THROUGH October 05, 1999.                          *
  *                                                             *
  *                                                             *
  * * * * * * * * * * * * * * * * * * * * * * * * * * * * * * *

=> s (pll or phase (2a) loop or synthesizer)(1p)(reference(8a)(loss or lost
or deviat? or window or range))

         10085 PLL
        496785 PHASE
        233386 LOOP
         18030 SYNTHESIZER
       1653885 REFERENCE
        361928 LOSS
        163485 LOST
        163912 DEVIAT?
        143919 WINDOW
       1019846 RANGE
L1         859 (PLL OR PHASE (2A) LOOP OR SYNTHESIZER)(1P)(REFERENCE(8A)(L
OSS
                OR LOST OR DEVIAT? OR WINDOW OR RANGE))

=> s l1 and (monitor? or detect? or sens?)(7a)(reference or input)

        302524 MONITOR?
        568893 DETECT?
        766905 SENS?
       1653885 REFERENCE
        549047 INPUT
        178832 (MONITOR? OR DETECT? OR SENS?)(7A)(REFERENCE OR INPUT)
L2         625 L1 AND (MONITOR? OR DETECT? OR SENS?)(7A)(REFERENCE OR INPU
T)

=> s l2 and frequency(5a)(range or window)

        394211 FREQUENCY
       1019846 RANGE
        143919 WINDOW
         58527 FREQUENCY(5A)(RANGE OR WINDOW)
L3         377 L2 AND FREQUENCY(5A)(RANGE OR WINDOW)

=> s l3 and (reference  or input)(7a)(deviat? or loss or lost)

       1653885 REFERENCE
        549047 INPUT
        163912 DEVIAT?
        361928 LOSS
        163485 LOST
         16878 (REFERENCE  OR INPUT)(7A)(DEVIAT? OR LOSS OR LOST)
L4         106 L3 AND (REFERENCE  OR INPUT)(7A)(DEVIAT? OR LOSS OR LOST)

=> s l4 and pll

         10085 PLL
L5          62 L4 AND PLL
```

=> d cit,ab 1-62

```
* * * * * * * * * * * * * * * * * * * * * * * * * * * * * *
  *                       G P I                              *
  *    J A P A N E S E   P A T E N T   A B S T R A C T S     *
  *                                                          *
  *    THE FILE IS CURRENT THROUGH APRIL 31, 1999.           *
  * * * * * * * * * * * * * * * * * * * * * * * * * * * * * *
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```
=>s 15

          8679 PLL
        168448 PHASE
         40183 LOOP
          6964 SYNTHESIZER
        166445 REFERENCE
         66516 LOSS
          9153 LOST
         70296 DEVIAT?
         55017 WINDOW
        236611 RANGE
           105 (PLL OR PHASE (2A) LOOP OR SYNTHESIZER)(1P)(REFERENCE(8A)(L
OSS
                OR LOST OR DEVIAT? OR WINDOW OR RANGE))
         95507 MONITOR?
        755683 DETECT?
        387519 SENS?
        166445 REFERENCE
        417510 INPUT
         69333 (MONITOR? OR DETECT? OR SENS?)(7A)(REFERENCE OR INPUT)
        245287 FREQUENCY
        236611 RANGE
         55017 WINDOW
          8197 FREQUENCY(5A)(RANGE OR WINDOW)
        166445 REFERENCE
        417510 INPUT
         70296 DEVIAT?
         66516 LOSS
          9153 LOST
          5399 (REFERENCE  OR INPUT)(7A)(DEVIAT? OR LOSS OR LOST)
          8679 PLL
```

```
* * * * * * * * * * * * * * * * * * * * * * * * * * * * * * * *
  *                     G P I                                  *
  *     E U R O P E A N   P A T E N T   A B S T R A C T S      *
  * * * * * * * * * * * * * * * * * * * * * * * * * * * * * * * *


=> s 15

          1207 PLL
         90334 PHASE
         38534 LOOP
          2295 SYNTHESIZER
         56818 REFERENCE
         20336 LOSS
          5570 LOST
         13626 DEVIAT?
         32486 WINDOW
         90374 RANGE
            61 (PLL OR PHASE (2A) LOOP OR SYNTHESIZER)(1P)(REFERENCE(8A)(L
OSS
                OR LOST OR DEVIAT? OR WINDOW OR RANGE))
         59628 MONITOR?
        174174 DETECT?
        177326 SENS?
         56818 REFERENCE
        111567 INPUT
         16355 (MONITOR? OR DETECT? OR SENS?)(7A)(REFERENCE OR INPUT)
         91124 FREQUENCY
         90374 RANGE
         32486 WINDOW
          5196 FREQUENCY(5A)(RANGE OR WINDOW)
         56818 REFERENCE
        111567 INPUT
         13626 DEVIAT?
         20336 LOSS
          5570 LOST
          1151 (REFERENCE  OR INPUT)(7A)(DEVIAT? OR LOSS OR LOST)
          1207 PLL
L6           0 L4 AND PLL
```

40. 4,901,033, Feb. 13, 1990, **Frequency** synthesizer with dynamically programmable **frequency range** of selected loop bandwith; Barry W. Herold, et al., 331/1A, 2, 8, 14, 17 [IMAGE AVAILABLE]

US PAT NO: 4,901,033 [IMAGE AVAILABLE] L5: 40 of 62

ABSTRACT:
A frequency **synthesizer** which includes at least one **phase** lock **loop** operative in a selected loop bandwidth state includes a dynamically programmable control circuit for setting the **frequency range** of its selected loop bandwidth state. In another aspect, the frequency **synthesizer** may include a plurality of **phase** lock **loop** circuits; and a common bias circuit programmably operative to generate at least one bias signal which is coupled commonly to the plurality of **phase** lock **loop** circuits for setting a common **frequency range** for the loop bandwidth states of all of the **phase** lock **loop** circuits. In still another aspect, the frequency **synthesizer** includes a **phase** lock **loop** circuit; and a bias circuit programmably operative to generate at least one bias signal which is coupled to the **phase** lock **loop** circuit for setting a **reference frequency range** of the loop bandwidth states thereof, the **phase** lock **loop** circuit being dynamically programmable to vary the **frequency range** settings of the loop bandwidth states in relation to the **reference frequency range** s

4. 5,719,508, Feb. 17, 1998, Loss of lock detector for master timing generator, William George Daly, 327/12, 2, 20, 39, 150, 156, 159; 331/1A, 25, DIG.2 [IMAGE AVAILABLE]

US PAT NO: 5,719,508 [IMAGE AVAILABLE] L5: 14 of 62

ABSTRACT:
A digital loss of lock detection (LLD) device for a **phase** looked **loop** (**PLL**) generates a locked frequency signal synchronized with a reference frequency signal. The LLD comprises first to fifth latching means for **detecting** when the **reference** clock failed high/low, when the locked clock failed high/low and when the **reference** clock is outside the tracking **range** of the **PLL**. The first to fifth latching means provide respectively a first to fifth error signals for e

7. 5,903,748, May 11, 1999, Method and apparatus for managing failure of a system clock in a data processing system; Kelvin E. McCollough, et al., 713/503; 714/47 [IMAGE AVAILABLE]

US PAT NO: 5,903,748 [IMAGE AVAILABLE] L5: 7 of 62

ABSTRACT:
Under software control, a loss of clock detect circuit (24) can be enabled to detect loss of clock. A plurality of different clock signals, including the input reference clock (34) to the **PLL** (12) and the feedback (36) from the **PLL** (12), are monitored by the loss of clock circuit (24). When the currently selected system clock (38) signal is lost, a control circuit (28) can select an optimal back-up clocking mode based on which clock signals were lost. One such selectable mode is to utilize the input reference clock (34) directly instead of the **PLL** (12). Another such selectable mode is to utilize the **PLL** (12) in a s

31. 5,168,245, Dec. 1, 1992, Monolithic digital phaselock loop circuit having an expanded pull-in range; Gregory N. Koskowich, 331/1A, 11, 14, 17, 25 [IMAGE AVAILABLE]

US PAT NO: 5,168,245 [IMAGE AVAILABLE] L5: 31 of 62

ABSTRACT:
A monolithic phaselock loop circuit (**PLL**) for controlling the phase and frequency of a VCO to compensate for process induced variations in the VCO natural frequency and to extend the pull-in **range** by .+-.50% of the **frequency** of a **reference** clock. The **PLL** is comprised of a VCO, a digital phase comparator, a digital frequency divider and a digital sequential phase error detector (SPED). The SPED circuit comprises two up-down counters, one to control the phase; the other, the frequency; a first one-shot circuit that drives the phase up-down counter to **detect** every level transition of the **reference** clock and a second one-shot circuit that drives the frequency up-down counter to provide a pulse for every falling edge of the reference clock; and a shift register responsive to the phase comparator to store the value of the phase comparator thereby providing indication of a frequency lock b

19. 5,561,390, Oct. 1, 1996, Clock signal generation circuit having **detective** circuit **detecting loss** of **reference** clock; Yasunori Hiiragizawa, 327/147, 20, 156 [IMAGE AVAILABLE]

US PAT NO: 5,561,390 [IMAGE AVAILABLE] L5: 19 of 62

ABSTRACT:
A clock signal generation circuit is disclosed which receives a **reference** clock and **detects**, in response thereto, the **loss** of the **reference** clock. A phase comparator 13, **detects** the phase difference between the **reference** clock signal and an stabilized clock from a **PLL synthesizer**, a signal DOWNB state of the phase comparator 13 is fixed to "0" level at the time of **loss** of the **reference** clock signal where the **reference** clock can be fixed to "0" or "1" level. The signal DOWNB is **monitored** using a **reference** clock **loss detection** circuit 12. If the signal DOWNB stays at the "0" level for a prescribed length of time, the **reference** clock **loss detection** circuit 12 judges that the **reference** clock is

18. 5,572,167, Nov. 5, 1996, Method and apparatus for a phase-locked loop circuit with holdover mode; John M. Alder, et al., 331/2; 327/156, 159; 331/1A, 14, 17, 25, 49; 375/376 [IMAGE AVAILABLE]

US PAT NO: 5,572,167 [IMAGE AVAILABLE] L5: 18 of 62

ABSTRACT:
A **phase**-looked **loop** circuit with holdover mode is formed utilizing a primary and secondary **phase**-locked **loop** circuits. Each loop circuit comprises a **phase** detector, **loop** filter, VCXO and frequency divider. The secondary loop is configured such that its output is very stable. The primary **loop** is **phase**-locked on a received reference clock signal and the second **loop** is **phase** locked on the output of the primary loop. The scaled output of the secondary loop being parallel to the reference clock signal. If the incoming **reference** signal is interrupted or **lost** the circuit is switched to a holdover mode where the input of the primary loop is switched to the stable scaled output of the secondary loop. In holdover mode, the output of the primary **loop** is **phase**-looked to the stable output of the secondary loop. When the reference clock signal is reestablished, the input of the primary loop is switched back to the r